AMENDMENTS

This section presents changes to the specification and the claims in a clean-unmarked format. A version with markings to show the changes made by the current amendment is provided after the remarks section.

In the Claims:

Presented below are the claims in a clean-unmarked format. Please cancel claims 17 and 20-44 without prejudice. Please add new claims 45-84 as follows:

Presentation Of The Claims In A Clean-Unmarked Format

45. (New) A method of forming an interconnect structure, comprising:

forming a first layer of a first dielectric material on a substrate;

patterning the first layer;

depositing conductive material over the patterned first layer;

planarizing the conductive material such that a plurality of interconnect lines are formed including a first and a second power interconnect lines and a third and fourth signal interconnect lines;

forming a mask layer over the interconnect lines and patterned first layer;

patterning the mask layer such that the first and second power interconnect lines and a first portion of the patterned first layer are covered, and the third and fourth signal interconnect lines and a second portion of the patterned first layer are uncovered;

removing the second portion of the patterned dielectric material of the first layer from the uncovered portion;

removing the patterned mask layer; and

depositing a second layer of a second dielectric material between the third and fourth signal interconnect lines, the second dielectric material having a smaller dielectric constant than the first dielectric material.

46. (New) The method of claim 45:

wherein the second dielectric material comprises a material having a dielectric constant that is less than that of silicon dioxide; and

wherein the first dielectric material comprises a material having a dielectric constant that is greater than or equal to that of silicon dioxide.

47. (New) The method of claim 46, wherein the first dielectric material has a dielectric constant that is greater than that of silicon dioxide.

48. (New) The method of claim 45:

wherein the second dielectric material comprises a material that is selected from the group consisting of an organic polymer, a nanofoam, a silicon based insulator containing an organic polymer, and a fluorine containing oxide of silicon; and

wherein the first dielectric material comprises barium strontium titinate.

49. (New) A microelectronic device comprising an interconnect structure formed by the method of claim 45.

50. (New) A method of forming an interconnect structure, comprising:

forming a first layer of a conductive material on a substrate;

forming a first pair of power interconnect lines to distribute power and a second pair of signal interconnect lines to carry signals from the conductive material;

depositing a first dielectric material over and between the first pair and the second pair;

forming a mask layer over the first pair and the second pair and first dielectric material;

patterning the mask layer such that one portion of the dielectric material between one pair is covered and another portion of the dielectric material between another pair is uncovered;

removing the portion of the dielectric material that is uncovered;

removing the patterned mask layer; and

depositing a second dielectric material having a different dielectric constant than a dielectric constant of the first dielectric material.

51. (New) The method of claim 50, wherein the first dielectric material has a dielectric constant that is greater than that of silicon dioxide and wherein the second dielectric material has a dielectric constant that is less than that of silicon dioxide.

52. (New) The method of claim 50, wherein the second dielectric material has a dielectric constant that is greater than that of silicon dioxide and wherein the first dielectric material has a dielectric constant that is less than that of silicon dioxide.

53. (New) The method of claim 50, wherein the one pair that is covered comprises the first pair of power interconnect lines and wherein the second dielectric material has a lower dielectric constant than the first dielectric material.

54. (New) The method of claim 50, wherein the one pair that is covered comprises the second pair of signal interconnect lines and wherein the second dielectric material has a higher dielectric constant than the first dielectric material.

55. (New) A microelectronic device comprising an interconnect structure formed by the method of claim 50.

56. (New) A method of making in-plane decoupling capacitors, comprising:

forming a first plurality of conductive power lines on an insulating substrate, the first plurality of conductive power lines having a first dielectric therebetween; and

forming a second plurality of conductive signal lines on the insulating substrate, the second plurality of conductive signal lines having a second dielectric therebetween;

wherein the first dielectric has a dielectric constant greater than a dielectric constant of the second dielectric.

57. (New) The method of claim 56:

wherein the second dielectric has a dielectric constant that is less than that of silicon dioxide; and

wherein the first dielectric has a dielectric constant that is greater than or equal to that of silicon dioxide.

58. (New) The method of claim 57, wherein the first dielectric has a dielectric constant that is greater than that of silicon dioxide.

59. (New) The method of claim 56:

wherein the second dielectric comprises a low dielectric constant material; and

wherein the first dielectric comprises a high dielectric constant material.

60. (New) The method of claim 59:

wherein the low dielectric constant material comprises a material that is selected from the group consisting of an organic polymer, a nanofoam, a silicon based insulator containing an organic polymer, and a fluorine containing oxide of silicon; and

wherein the high dielectric constant material comprises barium strontium titinate.

61. (New) The method of claim 56:

further comprising forming a third plurality of conductive lines on the insulating substrate, the third plurality of conductive lines having a third dielectric therebetween;

wherein the third dielectric has a different dielectric constant than that of the first and the second dielectrics; and

wherein the dielectric constant of the third dielectric is based on whether the third plurality of conductive lines are power lines or signal lines and based on the separation between the third plurality of conductive lines.

62. (New) A microelectronic device comprising an insulting substrate having formed thereon in-plane decoupling capacitors made by the method of claim 56.

63. (New) A method of forming an interconnect structure, comprising:

forming, on a substrate, a first plurality of signal interconnect lines and a first intralayer dielectric disposed between the first plurality of signal interconnect lines;

removing a portion of the first intralayer dielectric;

forming a second intralayer dielectric on the substrate where the first intralayer dielectric was removed; and

forming a second plurality of power interconnect lines in the second intralayer dielectric.

64. (New) The method of claim 63, wherein a dielectric constant of the first intralayer dielectric is different from a dielectric constant of the second intralayer dielectric.

65. (New) The method of claim 63:

wherein the second dielectric material comprises a low dielectric constant material; and

wherein the first dielectric material comprises a high dielectric constant material.

66. (New) The method of claim 65:

wherein the low dielectric constant material comprises a material that is selected from the group consisting of an organic polymer, a nanofoam, a silicon based insulator containing an organic polymer, and a fluorine containing oxide of silicon; and

wherein the high dielectric constant material comprises barium strontium titinate.

67. (New) The method of claim 63, wherein forming the second plurality of power interconnect lines comprises etching trenches in the second intralayer dielectric,

depositing a conductive material, and polishing the conductive material such that the conductive material is substantially removed except for that which is in the trenches.

68. (New) A microelectronic device comprising a substrate having an interconnect structure formed thereon by the method of claim 63.

69. (New) A method of forming an interconnect structure, comprising:

forming a first dielectric layer on a substrate;

removing a portion of the first dielectric layer;

forming a second dielectric layer on the substrate where the portion of the first dielectric layer was removed; and

forming a plurality of signal lines in the first dielectric layer and a power line in the second dielectric layer.

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70. (New) The method of claim 69, wherein a dielectric constant of the first dielectric is different from a dielectric constant of the second dielectric.

71. (New) The method of claim 70, wherein forming the plurality of signal lines and the power line comprises etching trenches in the first and the second dielectrics, depositing a conductive material, and polishing the conductive material such that the conductive material is substantially removed except for that which is in the trenches.

72. (New) The method of claim 69:

wherein the second dielectric layer comprises a low dielectric constant material; and

wherein the first dielectric layer comprises a high dielectric constant material.

73. (New) A microelectronic device comprising an interconnect structure formed by the method of claim 69.

74. (New) A method comprising:

providing a substrate; and

making on the substrate an interconnect structure comprising a first pair of interconnect lines to distribute power having a first dielectric material disposed therebetween and a second pair of interconnect lines to carry signals having a second dielectric material disposed therebetween, wherein the first dielectric material has a first dielectric constant that is greater than a second dielectric constant of the second material.

75. (New) The method of claim 74, wherein the second material comprises a low dielectric constant material.

76. (New) The method of claim 75, wherein the first material comprises a high dielectric constant material.

77. (New) The method of claim 76:

wherein the low dielectric constant material comprises a material that is selected from the group consisting of an organic polymer, a nanofoam, a silicon based insulator containing an organic polymer, and a fluorine containing oxide of silicon; and

wherein the high dielectric constant material comprises barium strontium titinate.

78. (New) The method of claim 74, wherein making further comprises making an interconnect structure comprising a third pair of interconnect lines having a third dielectric material disposed therebetween, wherein the third dielectric material has a third dielectric constant that is different than the first and the second dielectric constants.

79. (New) The method of claim 74, wherein the first pair of interconnect lines and the second pair of interconnect lines are separated by the same distance.

80. (New) The method of claim 74, wherein making includes removing a portion of the second material deposited between the first pair of interconnect lines and depositing the first material where the second material was removed.

81. (New) The method of claim 74, wherein making comprises protecting a second portion of the second material between the second pair of interconnect lines with a mask.

82. (New) The method of claim 74, wherein making includes removing a portion of the first material deposited between the second pair of interconnect lines and depositing the second material where the first material was removed.

83. (New) The method of claim 82, wherein making comprises protecting a second portion of the second material between the second pair of interconnect lines with a mask.

84. (New) A microelectronic device comprising an interconnect structure made by the method of claim 74.